



# SY58020U

## 6GHz, 1:4 CML Fanout Buffer/Translator with Internal I/O Termination

### General Description

The SY58020U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 CML fanout buffer. Optimized to provide four identical output copies with less than 15ps of skew and 27fs<sub>RMS</sub> of typical additive phase jitter, the SY58020U can process clock signals as fast as 6GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to differential LVPECL, LVDS, and CML signals (AC- or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage ( $V_{REF-AC}$ ) is provided to bias the  $V_T$  pin. The outputs are optimized to drive 400mV typical swing into 50Ω loads, with extremely fast rise/fall times guaranteed to be less than 60ps.

The SY58020U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require LVPECL outputs, consider the SY58021U or SY58022U 1:4 fanout buffer with 800mV and 400mV output swing, respectively. The SY58020U is part of Micrel's high-speed, Precision Edge® product line. Datasheets and support documentation are available on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

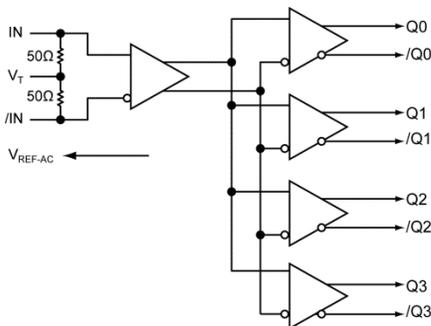
### Features

- Precision 1:4, 400mV CML fanout buffer
- Guaranteed AC performance over temperature/voltage:
  - > 6GHz  $f_{MAX}$  clock
  - < 60ps  $t_r / t_f$  times
  - < 250ps  $t_{pd}$
  - < 15ps max. skew
- Low-jitter performance:
  - 27fs<sub>RMS</sub> typical additive phase jitter
- Accepts an input signal as low as 100mV
- Unique patented input termination and  $V_T$  pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML
- 50Ω source terminated CML outputs
- Power supply 2.5V ±5% and 3.3V ±10%
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

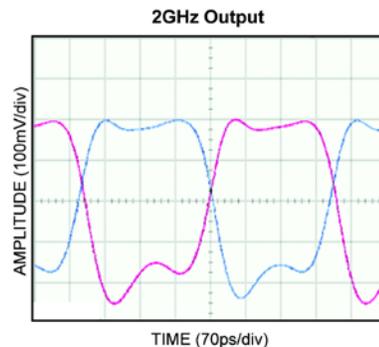
### Applications

- All SONET and All GigE clock distribution
- Fibre Channel clock and data distribution
- Backplane distribution
- Data distribution: OC-48, OC-48+FEC, XAUI
- High-end, low skew, multiprocessor synchronous clock distribution

### Functional Block Diagram



### Typical Performance



Precision Edge is a trademark of Micrel, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax +1 (408) 474-1000 • <http://www.micrel.com>

October 27, 2014

Revision 5.0  
[tcghelp@micrel.com](mailto:tcghelp@micrel.com) or (408) 955-1690

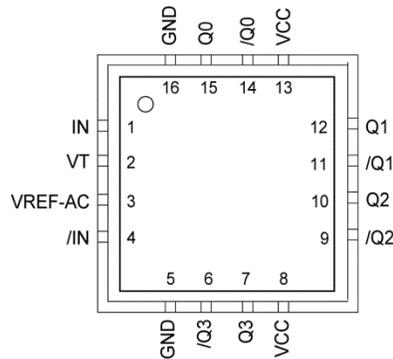
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58020UMG	QFN-16	Industrial	020U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58020UMG TR <sup>(2)</sup>	QFN-16	Industrial	020U with Pb-Free bar-line indicator	Pb-Free NiPdAu

### Note:

- Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC electrical only.
- Tape and Reel.

## Pin Configuration



16-Pin QFN (QFN-16)

## Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair receives the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the V <sub>T</sub> pin. Note that this input will default to an indeterminate state if left open. See “ <i>Input Interface Applications</i> ” section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The V <sub>T</sub> pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See “ <i>Input Interface Applications</i> ” section.
3	VREF-AC	Reference Output Voltage: This output biases to V <sub>CC</sub> -1.2V. It is used when AC-coupling to differential inputs. Connect V <sub>REF-AC</sub> directly to the V <sub>T</sub> pin. Bypass with 0.01μF low ESR capacitor to V <sub>CC</sub> . See “ <i>Input Interface Applications</i> ” section.
8, 13	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to the pins as possible.
5, 16	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15 11, 12 9, 10 6, 7	/Q0, Q0, /Q1, Q1, /Q2, Q2, /Q3, Q3	CML Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 400mV into 50Ω load. Normally terminate CML output pairs with 100Ω across Q and /Q outputs at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See “ <i>CML Output Termination</i> ” section.

**Absolute Maximum Ratings<sup>(3)</sup>**

Power Supply Voltage ( $V_{CC}$ )	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC}$
CML Output Voltage ( $V_{OUT}$ )	$V_{CC}-1.0V$ to $V_{CC}+0.5V$
Current ( $V_T$ )	
Source or sink current on $V_T$ pin	$\pm 100mA$
Input Current	
Source or sink current on IN, /IN	$\pm 50mA$
Current ( $V_{REF}$ )	
Source or sink current on $V_{REF-AC}$ <sup>(6)</sup>	$\pm 1.5mA$
Lead Temperature Soldering, (20 sec.)	260°C
Storage Temperature Range ( $T_S$ )	-65°C to +150°C

**Operating Ratings<sup>(4)</sup>**

Supply Voltage ( $V_{CC}$ )	+2.375V to +3.60V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Thermal Resistance	
QFN ( $\theta_{JA}$ )	
Still-Air	60°C/W
500lfpm	54°C/W
QFN ( $\Psi_{JB}$ )	
(Junction-to-Board Resistance) <sup>(5)</sup>	33°C/W

**DC Electrical Characteristics<sup>(7)</sup>**

$T_A = -40^\circ C$  to  $+85^\circ C$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{CC}$	Power Supply Voltage	$V_{CC} = 2.5V$	2.375	2.500	2.625	V
		$V_{CC} = 3.3V$	3.000	3.300	3.600	V
$I_{CC}$	Power Supply Current	No Load, $V_{CC} = \text{max.}$ (include internal 50 $\Omega$ pull-up)		150	180	mA
$V_{IH}$	Input HIGH Voltage	Note 8	$V_{CC}-1.600$		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage		0		$V_{IH}-0.100$	V
$V_{IN}$	Input Voltage Swing	See Figure 1.	0.100		1.700	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing	See Figure 2.	0.200		3.400	V
$R_{IN}$	IN-to- $V_T$ Resistance		40	50	60	$\Omega$
$V_{REF-AC}$	Output Reference Voltage		$V_{CC}-1.300$	$V_{CC}-1.200$	$V_{CC}-1.100$	V
$V_{T\_IN}$	IN-to- $V_T$ Voltage				1.280	V

**CML DC Electrical Characteristics<sup>(7)</sup>**

$V_{CC} = 3.3V \pm 10\%$  or  $2.5V \pm 5\%$ ;  $R_L = 100\Omega$  across each output pair or equivalent;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{OH}$	Output HIGH Voltage		$V_{CC}-0.020$	$V_{CC}-0.010$	$V_{CC}$	V
$V_{OUT}$	Output Voltage Swing	See Figure 1.	325	400	500	mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	See Figure 2.	650	800	1000	mV
$R_{OUT}$	Output Source Impedance		40	50	60	$\Omega$

**Notes:**

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
- Due to the limited drive capability, use for input of the same package only.
- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- $V_{IH}$  (min) not lower than 1.2V.

## AC Electrical Characteristics

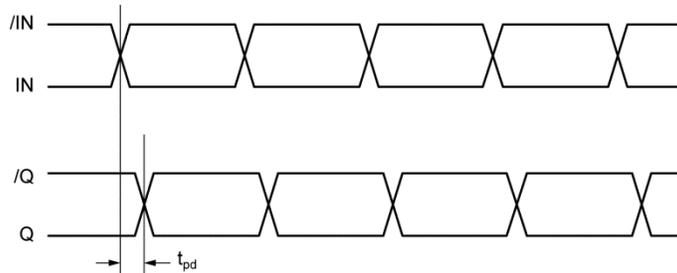
$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $R_L = 100\Omega$  across each output pair or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{MAX}$	Maximum Operating Frequency	$V_{OUT} \geq 200mV$ Clock	6			GHz
		NRZ Data		10		Gbps
$t_{pd}$	Propagation Delay		110	180	260	ps
$t_{SKEW}$	Output-to-Output Skew	Note 9		4	15	ps
	Part-to-Part Skew	Note 10			50	ps
$t_r, t_f$	Output Rise/Fall Time 20% to 80%	At full swing	20	40	60	ps
$t_{JITTER}$	Additive Phase Jitter	Carrier = 622MHz Integration Range: 12kHz – 20MHz		27		$f_{SRMS}$
		Carrier = 156.25MHz Integration Range: 12kHz – 20MHz		128		

**Notes:**

- 9. Skew is measured between outputs under identical transitions.
- 10. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

## Timing Diagram



## Single-Ended and Differential Swings

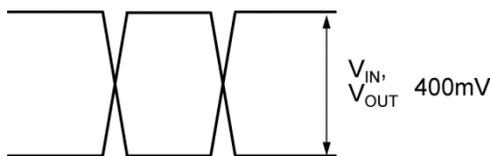


Figure 1. Single-Ended Voltage Swing

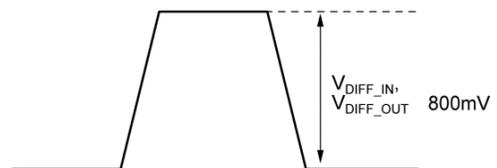
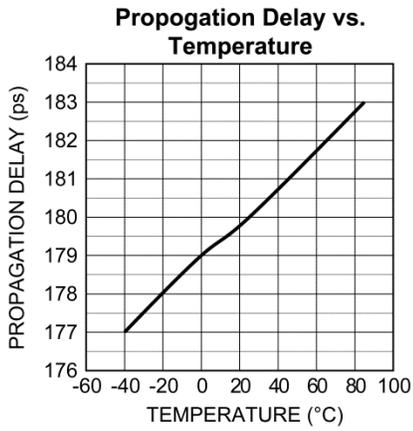
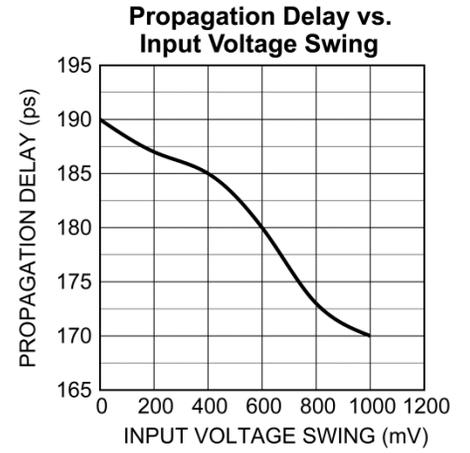
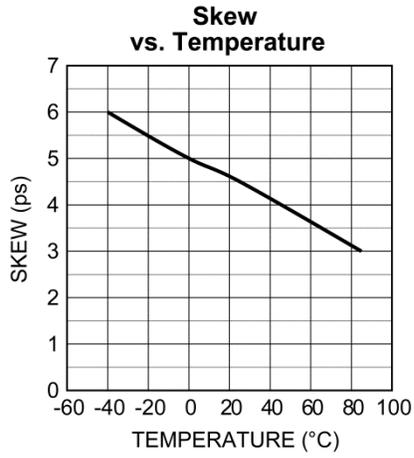
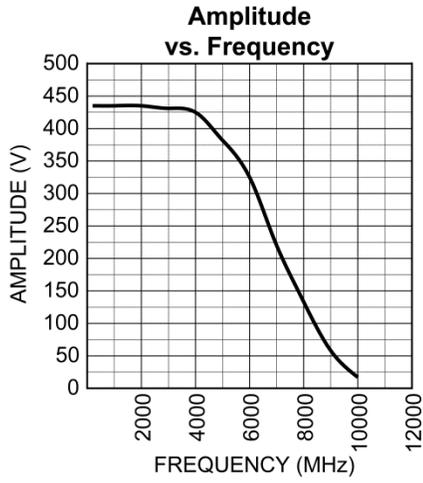


Figure 2. Differential Voltage Swing

## Typical Operating Characteristics

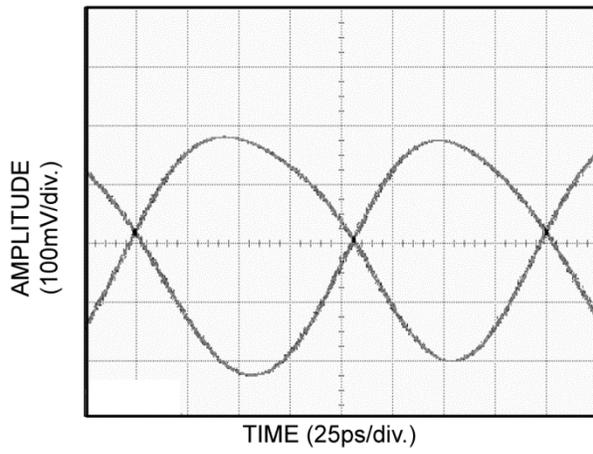
$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



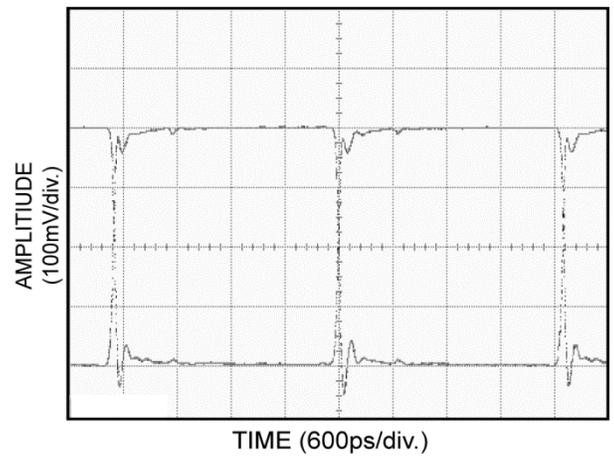
## Functional Characteristics

$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.

### 5GHz Output

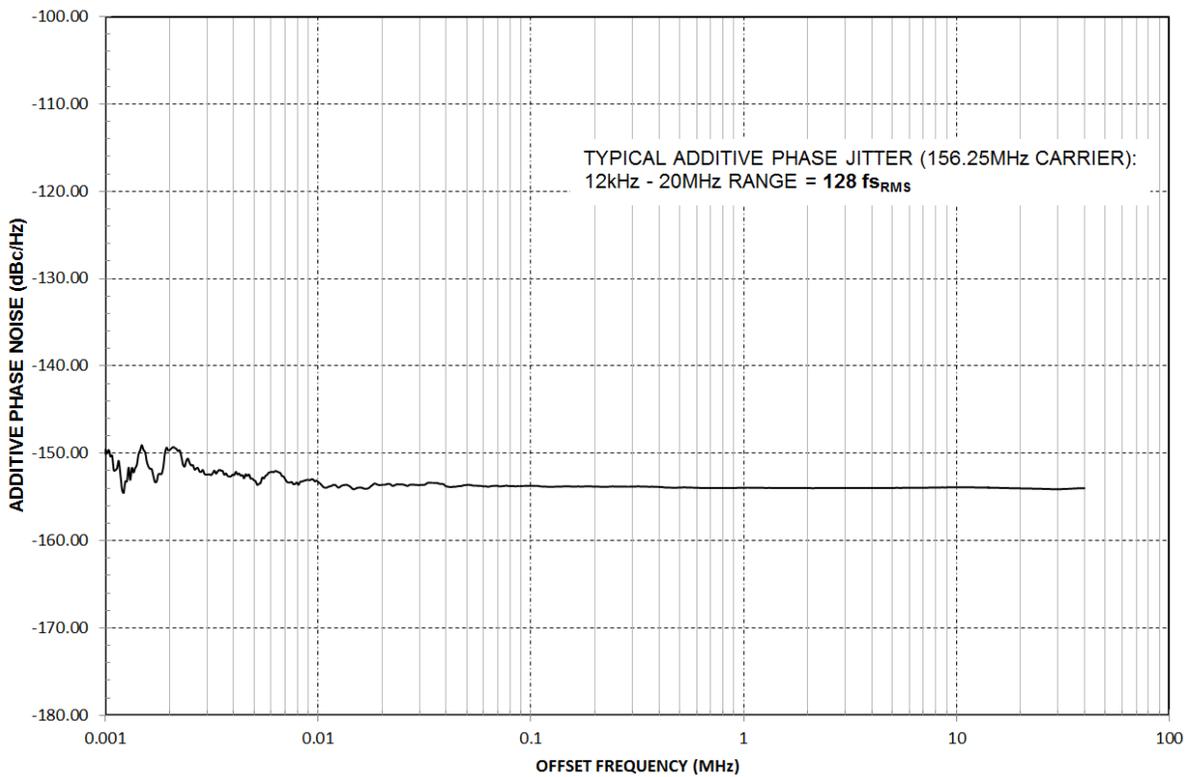
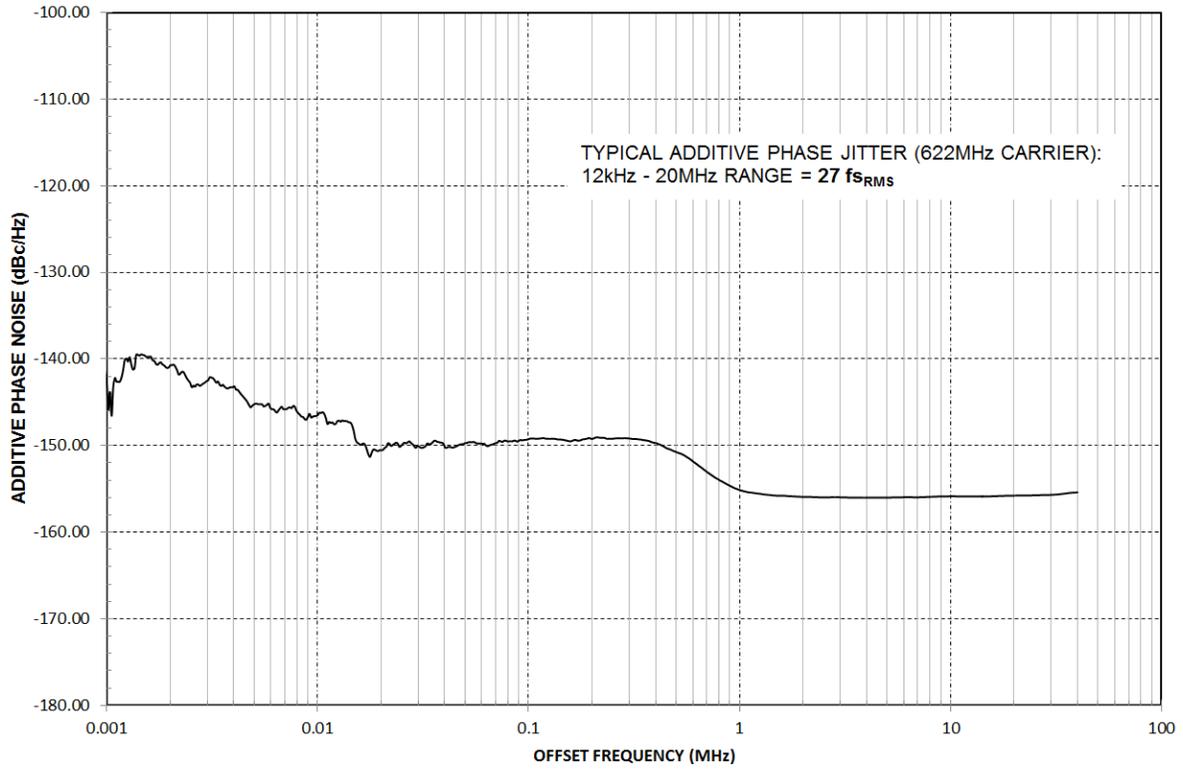


### 200MHz Output



### Additive Phase Noise Plots

V<sub>CC</sub> = 3.3V, GND = 0, T<sub>A</sub> = 25°C.



# Input Stage

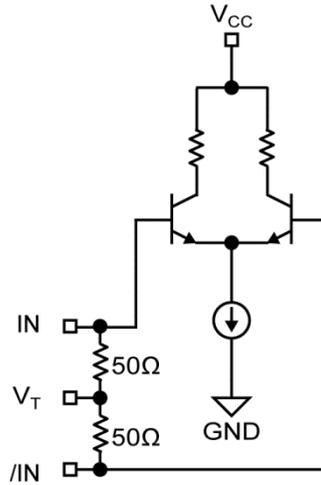


Figure 3. Simplified Differential Input Buffer

## Input Interface Applications

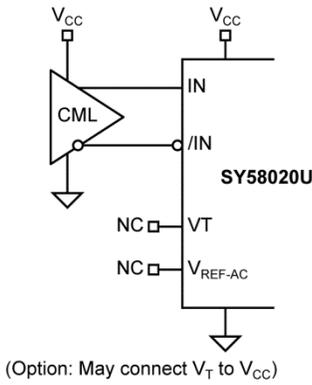


Figure 4. DC-Coupled CML Input Interface

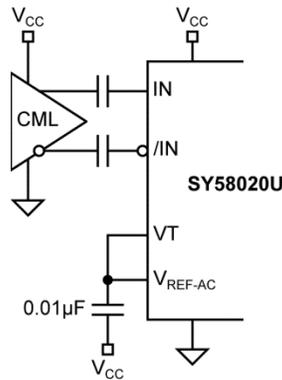


Figure 5. AC-Coupled CML Input Interface

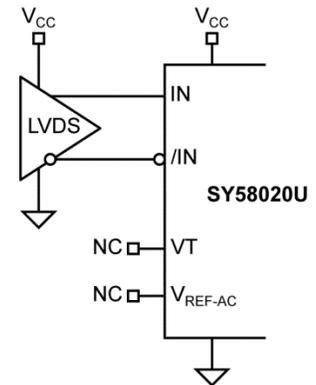


Figure 6. LVDS Input Interface

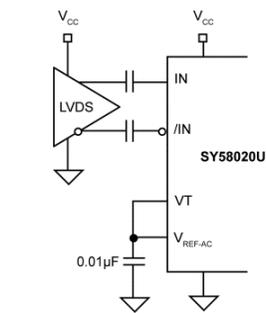


Figure 7. AC-Coupled LVDS Input Interface.

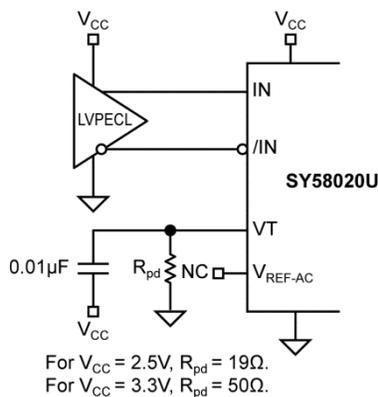


Figure 8. LVPECL Input Interface

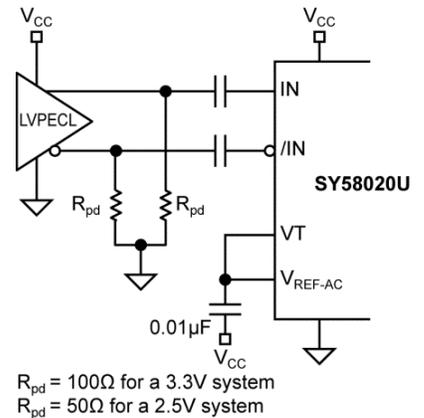


Figure 9. AC-Coupled LVPECL Input Interface

Note: Be certain that the LVDS driver can be AC-coupled.

## CML Output Termination

Figures 10 and 11 illustrate a CML output using both the AC-coupled and DC-coupled configuration. All outputs of the SY58020U are 50Ω with a 16mA current source.

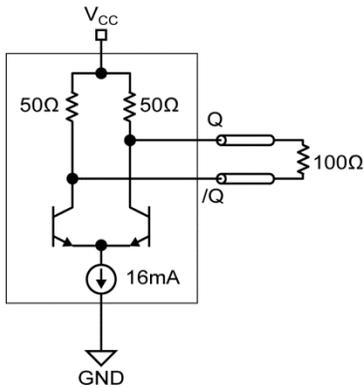


Figure 10. CML DC-Coupled

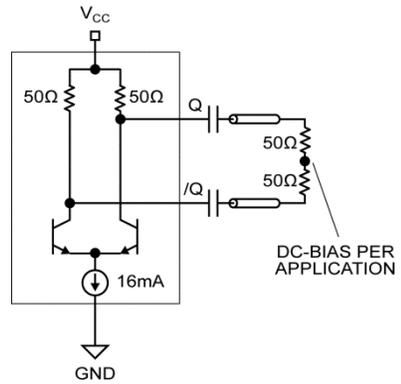
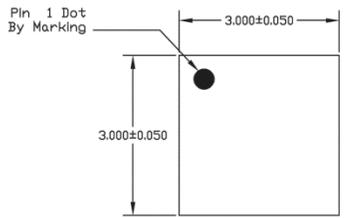
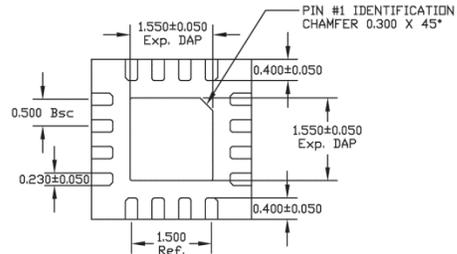


Figure 11. CML AC-Coupled Termination

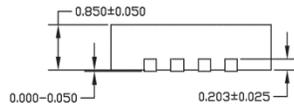
# Package Information<sup>(16)</sup>



TOP VIEW

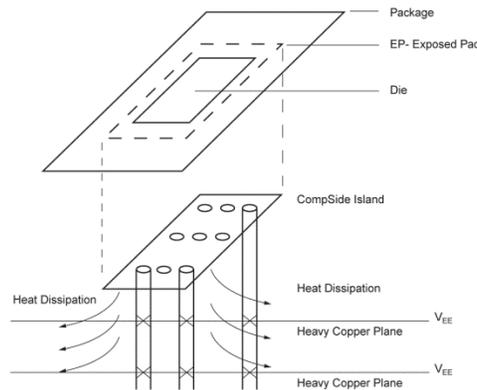


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 16-Pin QFN Package**  
(Always solder, or equivalent, the exposed pad to the PCB)

**Package Notes:**

- Note 1.** Package meets Level 2 qualification.
- Note 2.** All parts are dry-packaged before shipment.
- Note 3.** Exposed pads must be soldered to a ground for proper thermal management.

**16-Pin Package Type (QFN-16)**

**Note:**

11. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

---

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

Micrel, Inc. is a leading global manufacturer of IC solutions for the worldwide high performance linear and power, LAN, and timing & communications markets. The Company's products include advanced mixed-signal, analog & power semiconductors; high-performance communication, clock management, MEMs-based clock oscillators & crystal-less clock generators, Ethernet switches, and physical layer transceiver ICs. Company customers include leading manufacturers of enterprise, consumer, industrial, mobile, telecommunications, automotive, and computer products. Corporation headquarters and state-of-the-art wafer fabrication facilities are located in San Jose, CA, with regional sales and support offices and advanced technology design centers situated throughout the Americas, Europe, and Asia. Additionally, the Company maintains an extensive network of distributors and reps worldwide.

Micrel makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this datasheet. This information is not intended as a warranty and Micrel does not assume responsibility for its use. Micrel reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Micrel's terms and conditions of sale for such products, Micrel assumes no liability whatsoever, and Micrel disclaims any express or implied warranty relating to the sale and/or use of Micrel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2005 Micrel, Incorporated.

## Revision History

Date	Change Description/Edits by:	Rev.
8/4/10	Added new paragraph to disclaimer in boiler plate. Per Colin Sturt. M.Galvan	14
1/16/13	Complete rework	15
5/8/14	Updated Contact Email	16